REMARKS

This amendment is in response to the Office Action dated August 13, 2004. Reconsideration of the above-identified application in view of the amendments above and the following remarks is respectfully requested.

Claims 1-17 are currently pending in the application. Claims 1-17 have been rejected. Claims 1, 3-6 and 8 have been amended. Claim 2 has been cancelled. Claim 18 has been added.

Claims Rejections Under 35 USC 101

The Examiner rejected claims 1-17 over 35 USC 101 as lacking patentable utility. The Examiner states that the claims are directed to an abstract mathematical method and do not provide a real-world input or a tangible result.

Claim 1 as amended is now restricted to the field of design verification, and specifically to design verification by temporal analysis. Design verification is a crucial step in many industries. Design verification allows the designer of a system or device to ensure that a system meets specifications, during both system design and testing. Design verification enables the system designer to evaluate a design without the costly process of manufacturing and testing an actual device at every stage of the design process. Design verification also serves as a reliable way to ensure that an actual system performs as required.

As discussed extensively in the background of the present invention, the field of temporal analysis is known in the art. Temporal analysis of a system under test is performed by providing a temporal expression representing a specification of interest, and evaluating the response of the temporal expression to changes in specified system

variables. Typically, the evaluation of the temporal expression is performed using an abstract state machine or automaton which preserves the minimum necessary information at each state and in the transitions between states. System variable data is collected by sampling the values of various system variables at different times, either according to some triggering event or at predetermined times (see p. 4 lines 11-12). When the system variable data is input to the state machine, the state machine ends up in either a success or failure state. The designer can thus determine whether the system behavior is allowed by the specification.

The present invention provides a construction scheme for the conversion of a temporal expression (representing the behavior of a system) into a finite state machine having analyzable behavior (see the passage bridging pages 9 and 10). Such a construction scheme is lacking in the current art.

In order to focus the current invention clearly on the field of design verification using a finite state machine, and in light of the Examiner's comments, claim 1 is hereby amended to state:

> 1. A method for analyzing the temporal behavior of a system, the method comprising:
> inputting a specification for the temporal behavior of a system in the form of a temporal expression;
> parsing the temporal expression to form a hierarchical tree, each node of said hierarchical tree containing a subexpression of the temporal expression;
> propagating a sampling event to each node of said hierarchical tree according to at least one *Sampling* rule;
> forming a finite state machine by determining each transition from each node of said hierarchical tree to a successor node according to at least one transition Step rule to analyze the temporal expression;
> providing the values of a plurality of variables of said system sampled over a period of time to said finite state machine;
> evaluating the resulting state of said finite state machine to ascertain whether the resulting state comprises an error state; and
> providing an output indicating verification of a design of said system.

Claim 1 now clearly relates the invention to design verification of the temporal behavior of a system. The method is applicable to either a physical system or to a simulation, and it is respectfully submitted that the field of design verification of the temporal behavior of a system constitutes statutory subject matter. The applicability of the present invention to design verification is supported on p. 11 lines 5-14, which discusses the use of temporal expressions for describing the behavior of a device or concurrent system, for the purpose of design verification. The present invention is explicitly described as useful "for applications in which the dynamic properties of a system must be analyzed and evaluated". Claim 1 now clearly relates to a practical method which has a tangible result, that of providing a verified design. As such, the invention has utility in system development and testing.

Claim 1 now clearly specifies that the temporal expression describes the behavior of an actual system under test or of a system design. As discussed on page 12 lines 13-20, a temporal expression represents a set of finite sequences of defined states. The process of creating a temporal expression describing a system of interest is known in the art, and is discussed at length in the background section of the current application. The present invention expresses the set of sequences as a state machine whose evaluation leads to an "empty" set representing failure or to an "epsilon" state representing success.

The process of converting the temporal expression into a state machine which can be evaluated into either an "empty" or "epsilon" state is discussed in detail in the current application. In particular, the process of Tableau Construction based on sampling propagation is presented. Tableau construction results in a graph in which each node represents a partial evaluation of the given temporal expression (p. 17 line

22 to p. 18 line 2). At the end of the Tableau construction process, a state machine is formed which represents a complete evaluation of the temporal expression.

In addition, claim 1 now includes the step of providing samples of system variables over a period of time (i.e. system variable data). The samples are then fed into the automaton that results from the construction of the temporal expression. The finite state machine is then transversed to reach either a success state or a failure state. These steps are standard in the field of design verification by temporal analysis. The Applicant asserts that the present invention reaches the pre-computer processing safe harbor. The samples being processed in order to evaluate the state machine (which represents the temporal expression) are concrete, real-world measures of the parameters of a system of interest. For a physical system, the samples are obtained by performing measurements on a system or device. For a simulated system, the temporal expression must first be developed from a real-world system design. Only then can the sample values be determined.

The Examiner also objects that the Applicant has claimed a method without respect to the useful computing arts. The Applicant feels that claim 1 is now directed to the computer processing arts, since samples of system variables cannot be provided by mental activity *alone* but must be based on the performance of a given system or device.

In addition to the above, independent claim 18 is hereby added, which states:

> 18. A computer-readable storage medium containing a set of instructions for analyzing the temporal behavior of a system, comprising:
> a sample provision routine, for providing the values of a plurality of variables of said system sampled over a specified pattern in time;
> an expression formation input routine, for forming inputting a temporal expression from said values specifying the temporal behavior of a system;

a parsing routine, for parsing the temporal expression to form a hierarchical tree, each node of said hierarchical tree containing a subexpression of the temporal expression;
a propagation routing, for propagating a sampling event to each node of said hierarchical tree according to at least one Sampling rule; and
a transition determination state machine formation routine, for forming a finite state machine by determining each transition from each node of said hierarchical tree to a successor node according to at least one transition Step rule to analyze the temporal expression;
a sample provision routine, for providing the values of a plurality of variables of said system sampled over a period of time to said state machine;
a verification routine, for ascertaining whether said resulted in an error state of said finite state machine; and
an output routine, for providing an output indicating verification of a design of said system.

Support for the above is provided on page 8 lines 11-14, which indicates that the present invention may be implemented in software as a plurality of instructions performed by a data processor. As such, the invention may be defined as a group of data processing routines stored on a computer readable medium.

The Applicant believes that the current amendments make clear that the temporal expression being analyzed relates to a real-world system, and is not a purely mathematical construct. The present invention provides a construction methodology for construction of a finite state machine from a temporal expression representing a system of interest; a methodology which is lacking in current verification languages. System performance may thus be determined by evaluating the resulting state of the state machine to system variable data input, in order to verify that the system meets the required specifications.

No new matter is added by the present amendments.

All the matters raised by the Examiner have been dealt with.

In view of the foregoing, it is believed this application is now in condition for allowance, and an early Notice of Allowance is respectfully requested.

Respectfully submitted,

D'vorah Graeser
Agent for Applicant
Registration No. 40,000

Date: December 12, 2004